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Substitute for form 1449B/PTO			Complete if Known		
			Application Number	10/084,559	
	INFORMATION DISCL	_OSURE	Filing Date	2/25/2002	
STATEMENT BY APPLICANT			First Named Inventor	Pang et al	
	STATEMENT BY APP	LICANT	Art Unit	2616	
			Examiner Name	Mark Mais	
(Use as many sheets as necessary)					
Sheet	1 of	1	Attorney Docket Number	0037203-15	

	1	NON PATENT LITERATURE DOCUMENTS	1		21 71 2	_	
Examiner	Cite	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine,					
Initials*	No.	published.			er, city and/or country where		
	1	M.Weiss, F. Engel and G.P. Fettweis. A New Scalable DSP Architecture for					
		System on Chip (SOC) Domains. In IEEE International Conference on Acoustics,					
		Speech and Signal Processing (ICASSP), 1999.					
	2	Lyonnard et al., Automatic Generation of Application-Specific Architectures for					
		Heterogenous Multiprocessor System-on-Chip, June 2001, ACM Press,					
		Pages:518-523, Annual ACM IEEE Design Automation Conference.					
	3	Cuviello et al., Fault Modeling and Simulation for Cross in System on Chip					
		Interconnects, Computer-Aided Design, 1999. Digest of Technical Papers. 1999					
		IEEE/ACM International Conference, 7-11 Nov. 1999, Pages: 297-303					
	4	Papachristou et al., Microprocessor based testing for core-based system on chip,					
		1999. ACM Press, Annual ACM IEEE Design Automation Conference,					
		Proceedings of the 36 th ACM/IEEE conference on Design Automation, Pages:					
		586-591, ISBN: 1-58133-109-7.					
	5	Picone et al., Enhancing the Performance of Speech Recognition with Echo					
		Cancellation, 11-14 April 1988, Acoustics, Speech, and Signal Processing, 1988.					
		ICASSP-88, Pages: 529-532, vol. 1					
	6	Wang et al., Hardware/Software Instruction Set Configurability for System-on-Chip					
		Processors, June 2001, ACM Press, Annual ACM IEEE Design Automation					
		Conference, Pages:184-188, ISBN: 1-58113-297-2.					
	7	Lahiri et al, Fast Performance Analysis of Bus-Based System-On-Chip					
		Communication Architectures, 7-11 Nov. 1999, Pages:566-572, Computer-Aided					
		Design, 1999. Digest of Technical Papers. 1999 IEEE/ACM International					
		Conference.					
	8	Juarez et al., A VLSI Architecture for MPEG-4 Stream Processing and					
		Communication, Packet Video 2000, IEEE					
	9	Juarez et al, A System-on-a-Chip for Multimedia Stream Processing and					
		Communication, EUSIPCO 2000, International Society for Magnetic Resonance in					
		Medicine.					
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Examiner	r	Date			
Signature	Э	Considered			

^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.